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PHOTOELECTRIC LEAK CURRENT COMPENSATING CIRCUIT AND OPTICAL SIGNAL CIRCUIT USING SAME

FIELD OF THE INVENTION

The present invention relates to a photoelectric leak current compensating circuit that compensates for a photoelectric leak current of a Darlington circuit provided in an integrated circuit, and relates to an optical signal circuit including the photoelectric leak current compensating circuit, the optical signal circuit being provided in proximity with an electricity-light conversion element, such as a light emitting diode, or in proximity with a light-electricity conversion element, such as a photodiode.

BACKGROUND OF THE INVENTION

Some integrated circuits, such as receiving ICs in infrared remote controls, ICs for receiving optical pickup signals, and ICs for

driving LEDs, are provided in proximity with electricity-light conversion elements, such as LEDs, or in proximity with light-electricity conversion elements, such as photodiodes. In these integrated circuits, photoelectric currents are generated in parasitic photodiodes by diffracted light of signal light or scattered light of signal light, or by noise light of fluorescent lights and the like. Such photoelectric currents cause malfunction of circuits. Especially, in laterally structured transistors, because N-type epitaxial layers (base scattering regions in PNP transistors, and collector scattering regions in NPN transistors) have large areas, the photoelectric currents generated by the parasitic photodiodes increase base currents in the PNP transistors and collector currents in the NPN transistors. This significantly affects properties of the circuits. The following describes such a phenomenon with reference to Figs. 6 to 12.

Fig. 6 schematically illustrates a structure of a lateral PNP transistor 1. Fig. 7 illustrates an equivalent circuit of the lateral PNP transistor 1. On a P-type substrate layer 2, an N-type epitaxial layer 3 is provided. The N-type epitaxial layer 3 is separated by trenches 4 into element regions. Due to the structure of the integrated circuit, a parasitic photodiode 5 is generated between the N-type epitaxial layer 3, which is to be the base scattering region, and the substrate layer 2, and the parasitic photodiode 5 is connected between a base terminal of the PNP transistor 1 and the substrate layer 2 (ground).

Therefore, when an incidence of light generates a photoelectric current Ipd flowing from the N-type epitaxial layer 3 to the substrate layer 2, as shown in Fig. 6, the photoelectric current Ipd functions as a base current Ib of the PNP transistor 1, thereby significantly influencing the properties of the circuit. The photoelectric current Ipd becomes larger as an amount of incident light becomes larger. Therefore, the photoelectric current Ipd becomes large if the PNP transistor 1 is provided in proximity with a light-electricity conversion element. Also, the photoelectric current Ipd becomes larger as an area of the N-type epitaxial layer 3 becomes larger. Therefore, the photoelectric current Ipd becomes larger as a current capacity of the PNP transistor 1 becomes larger.

Likewise, Fig. 8 schematically illustrates a structure of a lateral NPN transistor 11, and Fig. 9 illustrates an equivalent circuit of the lateral NPN transistor 11. On a P-type substrate layer 12, an N-type epitaxial layer 13 is provided. The N-type epitaxial layer 13 is separated by trenches 14 into element regions. Between the N-type epitaxial layer 13, which is to be the collector scattering region, and the substrate layer 12, a parasitic photodiode 15 is generated, and the parasitic photodiode 15 is connected between a collector terminal of the PNP transistor 11 and the substrate layer 12 (ground).

Therefore, when an incidence of light generates a photoelectric current Ipd flowing from the N-type epitaxial layer 13 and the substrate layer 12, as shown in Fig. 8, a collector current of

the NPN transistor 11 decreases by the photoelectric current Ipd. This significantly influences the properties of the circuit. The photoelectric current Ipd becomes larger as an amount of incident light becomes larger, and as an area of the N-type epitaxial layer 13 becomes larger. However, the area of the N-type epitaxial layer 13 can be smaller in the NPN transistor 11 than in the PNP transistor 1, because the NPN transistor 11 has a greater current driving capability than that of the PNP transistor 1. Moreover, the generated photoelectric current influences the collector current. Therefore, it is considered that an influence of the photoelectric current Ipd is smaller in the NPN transistor 11 by a current amplification rate hfe than in the PNP transistor 1.

The influence of the photoelectric current is small also in a vertical transistor. A structure of a vertical transistor is described below, with reference to Figs. 10 and 11. Fig. 10 schematically illustrates a structure of a vertical PNP transistor 21. Fig. 11 is an equivalent circuit diagram of the vertical PNP transistor 21. As in the laterally structured transistors 1 and 21, on a P-type substrate layer 22, an N-type epitaxial layer 23 is provided, and the N-type epitaxial layer 23 is separated by trenches 24 into element regions. Although a parasitic photodiode 25 is generated between the P-type substrate layer 22 and the N-type epitaxial layer 23, only a predetermined electric potential (generally, a line voltage Vcc) is supplied to the N-type epitaxial layer 23, due to the structure of the vertical transistor. Therefore, the photoelectric leak current does

not influence operation of the transistor. There is also a parasitic photodiode 26 between a base scattering region (N) and the collector scattering region (P). However, because a base scattering area is small, an influence of the parasitic photodiode 26 on the vertical PNP transistor 21 is much smaller than the influence of the parasitic photodiode 5 on the lateral PNP transistor 1.

However, there are cases where it is structurally required to use a lateral transistor in order to reduce the number of masks, for example. Generally, a Darlington circuit, in which a collector of an NPN transistor is connected to a base of a PNP transistor, is often used in order to improve an input impedance. In the Darlington circuit, a photoelectric leak current generated at the collector of the NPN transistor becomes a base current of the PNP transistor. Therefore, the leak current causes a problem even if the vertical transistor is used.

Fig. 12 is an electrical diagram of such a Darlington circuit 31. An emitter of a PNP transistor qp1 is connected to a bias source such as a high level power source. A collector of the PNP transistor qp1 is an output terminal. A base of the PNP transistor qp1 is connected to a collector of an NPN transistor qn1, as described above. A base of the NPN transistor qn1 is an input terminal, and an emitter of the NPN transistor qn1 is connected to the output terminal.

A parasitic photodiode dp1 is generated at the base of the PNP transistor qp1, which includes the N-type epitaxial layer, and a

parasitic photodiode dn1 is generated at the collector of the NPN transistor qn1. Through the parasitic photodiodes dp1 and dn1, photoelectric leak currents i1 and i2 flow, respectively. Here, if it is assumed that areas of the N-type epitaxial layers of the PNP transistor qp1 and the NPN transistor qn1, that is, the base scattering region of the PNP transistor qp1 and the collector scattering region of the NPN transistor qn1, are s1 and s2, respectively, the photoelectric currents are given by i1=s1×Ipd(p), and i2=s2×Ipd(n), respectively, where Ipd(p) is an amount of the photoelectric leak current per unit area of the N-type epitaxial layer of the PNP transistor, and Ipd(n) is an amount of the photoelectric leak current per unit area of the N-type epitaxial layer of the NPN transistor.

Therefore, influences of the photoelectric leak currents i1 and i2 are multiplied by hfe at the PNP transistor qp1. From the output terminal, a photoelectric leak current Ileak is outputted. This significantly influences the circuit properties. The photoelectric leak current Ileak is as follows:

$$Ileak=hfe(p)\times\{s1\times Ipd(p)+s2\times Ipd(n)\} \quad ...(1)$$

where hfe(p) is a current amplification rate of the PNP transistor qp1.

As a method of decreasing the influences of the photoelectric leak currents generated by the parasitic photodiodes dp1 and dn1, there is a method in which surfaces of elements are covered with metal wires, so as to prevent light from coming in through the

surfaces of the elements. However, there are cases where the method is insufficient to prevent light from coming in through those portions that cannot be light-shielded, such as chip side surfaces and chip edges. Moreover, because reduction of chip areas and reduction of the number of masks are recently required to attain cost reduction, the light-shielding by using the metal wires cannot be performed sufficiently. Furthermore, the influences of the photoelectric leak currents generated by the parasitic photodiodes are relatively increasing because of lower power consumption to save energy.

To solve the problems above, proposed are photoelectric compensating circuits, which are typical related arts, described in Japanese Publication for Unexamined Patent Application, *Tokukaihei* No. 3-262153 (Publication Date: November 21, 1991) and Japanese Publication for Unexamined Patent Application, *Tokukaihei* No. 6-45536 (Publication Date: February 18, 1994). In these arts, photoelectric currents in base currents of such PNP transistors that are used alone are compensated for. Fig. 13 illustrates an example where these arts are applied to a Darlington circuit, in which an NPN transistor is used in combination with PNP transistors. In Fig. 13, portions corresponding to those in the structure of Fig. 12 are labeled with the same referential numerals, and explanations thereof are omitted.

A compensating circuit 32 includes PNP transistors qp11 and qp 12, and an NPN transistor qn11. An emitter of the PNP transistor

qp11 is connected to the bias source, such as a high level power source, and a collector of the PNP transistor qp11 outputs a compensating current io. A base of the PNP transistor qp11 is connected to a base and a collector of the PNP transistor qp12, which constitutes a current mirror circuit. An emitter of the PNP transistor qp12 is connected to the bias source, such as a high level power source, and a collector of the PNP transistor qp12 is connected to the base of the PNP transistor qp11 and to the collector of the NPN transistor qn11. The base and emitter of the NPN transistor qn11 are grounded.

Therefore, as described above, parasitic photodiodes dp11, dp12, and dn11 are respectively generated at the bases of the PNP transistors qp11 and qp 12, and the collector of the NPN transistor qn11. Through the parasitic photodiodes dp11, dp12, and dn11, photoelectric leak currents i3, i4, and i5 flow, respectively. Where areas of N-type epitaxial layers of the PNP transistors qp11 and qp12 and of the NPN transistor qn11, that is, base scattering regions of the PNP transistors qp11 and qp12 and a collector scattering region of the NPN transistor qn11, are s3, s4, and s5, respectively, the photoelectric leak currents are given by $i3=s3\times Ipd(p)$, $i4=s4\times Ipd(p)$, and $i5=s5\times Ipd(n)$.

Here, if the base currents of the transistors are disregarded, that is, if it is assumed that the current amplification rate $hfe\rightarrow\infty$,

$io(qp11)=(m1/m2)\times\{s5\times Ipd(n)+(s3+s4)\times Ipd(p)\}$ ...(2); and

$Ileak=hfe(p)\times[\{s1\times Ipd(p)+s2\times Ipd(n)\}$

$$-(m1/m2)\times\{s5\times Ipd(n)+(s3+s4)\times Ipd(p)\}] \quad ...(3)$$

where m1/m2 is a current ratio between the PNP transistors qp11 and qp12, which constitute the current mirror circuit.

Thus, the compensating circuit 32 is so arranged that the photoelectric leak currents i1 and i2, which are respectively generated at the parasitic photodiodes dp1 and dn1, are canceled by the photoelectric leak currents i3, i4, and i5, which are respectively generated at the parasitic photodiodes dp11, dp12, and dn11 of the transistors qp11, qp12 and qn11 in the compensating circuit 32.

However, in such related art, the photoelectric leak currents i1 and i2 can be completely canceled only if the following two equations are simultaneously satisfied:

$s2=(m1/m2)\times s5$ ...(4); and

$s1=(m1/m2)\times(s3+s4)$ ...(5).

Assuming that m1:m2=1:1, the two equations are simultaneously satisfied only if s1:s2:s3:s4:s5=2:1:1:1:1. Therefore, a total area of the N-type epitaxial layers needs to be equivalent to that of six transistors. This is problematic because the number of elements is increased, thereby increasing a chip area.

In the foregoing explanation, the influences of the base currents is disregarded, that is, it is assumed that $hfe\rightarrow\infty$, for the sake of simple explanation. However, there is a problem that, in general, an actual value of the current amplification rate hfe is around 100, and an influence thereof cannot be disregarded.

Generally, if the collector current is very weak, the current amplification rate hfe is small, whereby an influence of the base current is large. A current amplification rate hfe of a lateral PNP transistor is smaller than those of the lateral NPN transistor and the vertical PNP transistor. Therefore, the influences of the base currents are large.

If a base current Ib is taken into consideration, a relationship between the base current Ib and a collector current Ic in each transistor is given by:

$$Ib=Ic/hfe \quad ...(6).$$

Therefore, Equations (2) and (3) are expressed as the following Equations (7) and (8):

$$io(qp11)=\{hfe(p)/(hfe(p)+2)\} \times(m1/m2)\times\{s5\times Ipd(n)+(s3+s4)\times Ipd(p)\} \quad ...(7); \text{ and}$$

$$Ileak=(hfe(p)-1)\times[\{s1\times Ipd(p)+s2\times Ipd(n)\} -\{hfe(p)/(hfe(p)+2)\}\times(m1/m2) \times\{s5\times Ipd(n)+(s3+s4)\times Ipd(p)\}] \quad ...(8).$$

Therefore, such a compensating circuit is needed that decreases the influences of the photoelectric leak currents on the Darlington circuit more efficiently.

SUMMARY OF THE INVENTION

An object of the present invention is therefore to provide a photoelectric leak current compensating circuit capable of compensating for a photoelectric leak current of a Darlington circuit

with a high accuracy without increasing a chip area, and to provide an optical signal circuit using the photoelectric leak current compensating circuit.

To solve the problems above, a photoelectric leak current compensating circuit of the present invention is a photoelectric leak current compensating circuit for compensating for a photoelectric leak current generated in a Darlington circuit, which is provided in an integrated circuit, including a first PNP transistor and a second NPN transistor whose collector is connected to a base of the first PNP transistor, the photoelectric leak current compensating circuit including a Darlington circuit, including a third PNP transistor, whose emitter is connected to a collector of the first PNP transistor and whose collector is grounded, for compensating for the photoelectric leak current by absorbing a collector current of the first PNP transistor; and a diode-structured fourth NPN transistor whose collector is connected to a base of the third PNP transistor and whose base and emitter are connected to each other.

According to this arrangement, in order to compensate for the photoelectric leak current of the Darlington circuit (i) which is provided in the integrated circuit, (ii) in which the base of the first PNP transistor is connected to the collector of the second NPN transistor, and (iii) which is suitable for improving an input impedance, the compensating circuit includes the Darlington circuit including the third PNP transistor, whose emitter is connected to the collector of the first PNP transistor and whose collector is

grounded, and the diode-structured fourth NPN transistor whose collector is connected to the base of the third PNP transistor and whose base and emitter are connected to each other, the photoelectric leak current being compensated by absorption of the collector current of the first PNP transistor by the emitter of the third PNP transistor.

If the photoelectric leak current is compensated by using a base current of the first PNP transistor, as shown in Fig. 13, a current mirror circuit or the like is needed in order to add a compensating current to the base current. Therefore, the number of elements is increased, thereby increasing the chip area. In contrast, with the foregoing arrangement, the photoelectric leak current is compensated by using the collector current. This makes it possible to compensate for the photoelectric leak current with a high accuracy without increasing the chip area, by so disposing the compensating circuit and the Darlington circuit that the compensating circuit and the Darlington circuit are equally influenced by light (e.g. by disposing the compensating circuit and the Darlington circuit on the same integrated circuit and in proximity with each other), the Darlington circuit including the third PNP transistor and the fourth NPN transistor, which have N-type epitaxial layers of substantially identical areas.

For a fuller understanding of the nature and advantages of the invention, reference should be made to the ensuring detailed description taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is an electrical diagram of one embodiment of the present invention.

Fig. 2 is an electrical diagram of related art.

Fig. 3 is a block diagram of an electric discharge circuit of a wave detecting circuit as one example in which a Darlington circuit and a compensating circuit shown in Fig. 1 are used.

Fig. 4 is a block diagram illustrating an arrangement of a receiving device of an infrared remote control that uses, as the wave detecting circuit, the electric discharge circuit shown in Fig. 3.

Fig. 5 is an electrical diagram of another embodiment of the present invention.

Fig. 6 is a schematic diagram illustrating a structure of a lateral PNP transistor.

Fig. 7 is an equivalent circuit diagram of Fig. 6.

Fig. 8 is a schematic diagram illustrating a structure of a lateral NPN transistor.

Fig. 9 is an equivalent circuit diagram of Fig. 8.

Fig. 10 is a schematic diagram illustrating a structure of a vertical PNP transistor.

Fig. 11 is an equivalent circuit diagram of Fig. 10.

Fig. 12 is an electrical diagram of the Darlington circuit.

Fig. 13 is an electrical diagram illustrating the Darlington circuit of Fig. 12 where typical related art is applied.

DESCRIPTION OF THE EMBODIMENTS

With reference to Figs. 1 to 4, the following describes one embodiment of the present invention.

Fig. 1 is an electrical diagram of one embodiment of the present invention. In this circuit, a Darlington circuit 41, which improves an input impedance, is used as a compensation target circuit. The Darlington circuit 41 includes a PNP transistor (first PNP transistor) QP1 and an NPN transistor (second NPN transistor) QN1, which are provided on the same integrated circuit. The Darlington circuit 41 has the same arrangement as that of the Darlington circuit 31 in Fig. 12. An emitter of the PNP transistor QP1 is connected to a bias source such as a high level power source, a collector of the PNP transistor QP1 is used as an output terminal, and a base of the PNP transistor QP1 is connected to a collector of the NPN transistor QN1. A base of the NPN transistor QN1 is used as an input terminal, and an emitter of the NPN transistor QN1 is connected to the output terminal.

A compensating circuit (photoelectric leak current compensating circuit) 42 compensates for photoelectric leak currents I1 and I2, which are respectively generated by parasitic photodiodes DP1 and DN1 formed at N-type epitaxial layers, that is, at the base of the PNP transistor QP1 and the collector of the NPN transistor QN1, respectively. The compensating circuit 42 includes a Darlington circuit including, like the Darlington circuit 41, a PNP

transistor (third PNP transistor) QP11 and an NPN transistor (fourth NPN transistor) QN11. The Darlington circuit 41 and the compensating circuit 42 are so disposed in proximity with each other on the same integrated circuit as to be equally influenced by light. An emitter of the PNP transistor QP11 is connected to the collector of the PNP transistor QP1, a collector of the PNP transistor QP11 is grounded, and a base of the PNP transistor QP11 is connected to a collector of the NPN transistor QN11. A base and the collector of the NPN transistor QN11 are grounded.

Therefore, parasitic photodiodes DP11 and DN11 are respectively formed at the base of the PNP transistor QP11 and the collector of the NPN transistor QN11, which are made of the N-type epitaxial layers, and photoelectric leak currents I3 and I4, which are generated by the parasitic photodiodes DP11 and DN11, flow.

Where areas of base scattering regions of the PNP transistors QP1 and QP11 are S1 and S3, respectively, and areas of collector scattering regions of the NPN transistors QN1 and QN11 are S2 and S4, respectively, the base scattering regions being the N-type epitaxial layers of the PNP transistors QP1 and QP11, and the collector scattering regions being the N-type epitaxial layers of the NPN transistors QN1 and QN11, Ipd(p) is an amount of the photoelectric leak current per unit area of the N-type epitaxial layer of the PNP transistor, and Ipd(n) is an amount of the photoelectric leak current per unit area of the N-type epitaxial layer of the NPN transistor, the photoelectric leak currents are given by $I1=S1\times Ipd(p)$,

I2=S2×Ipd(n), I3=S3×Ipd(p), and I4=S4×Ipd(n).

Therefore, if influences of base currents of the transistors are disregarded for the sake of simplicity, that is, if it is assumed that hfe→∞, the output terminal outputs, according to Kirchhoff's law, the following current Iout:

$$\begin{aligned} Iout &= Ileak - Io \\ &= hfe(p)\times\{S1\times Ipd(p)+S2\times Ipd(n)\} \\ &\quad -hfe(p)\times\{S3\times Ipd(p)+S4\times Ipd(n)\} \quad \ldots(9) \end{aligned}$$

where hfe(p) is a current amplification rate of the PNP transistors QP1 and QP11, Ileak is a total amount of the photoelectric leak currents outputted from the collector of the PNP transistor QP1, and Io is a compensating current absorbed from the output terminal by the compensating circuit 42.

Therefore, the photoelectric leak current Ileak can be canceled by so arranging that S1=S3 and S2=S4. In this case, S1:S2:S3:S4=1:1:1:1. Therefore, a total area of the N-type epitaxial layers can be just enough to include four transistors, thereby preventing the increase of the chip area.

As described above, by using the collector current of the PNP transistor QP1 and by using the compensating circuit 42 including a Darlington circuit similar to the Darlington circuit 41, it is possible to compensate, with a high accuracy, for the photoelectric leak current Ileak generated at the Darlington circuit 41. For integrated circuits that cannot shut off light incoming from outside, this arrangement is very effective to increase accuracy while dealing

with very weak currents or operating under unignorable influences of parasitic photodiodes.

With the arrangement of Fig. 13, the current mirror circuit or the like is needed in order to add the compensating current io to the base current. Therefore, the number of elements is increased, thereby increasing the chip area. In contrast, if the photoelectric leak current is compensated by using the collector current, it is possible to prevent the increase of the chip area as described above, because the photoelectric leak current can be compensated by simply providing, to the compensating circuit 42, the PNP transistor QP11 and the NPN transistor QN11, which have N-type epitaxial layers having substantially identical areas.

In the foregoing explanation, it is so arranged that S1=S3 and S2=S4. That is, the areas of the N-type epitaxial layers of the transistors QP1 and QN1, which are provided to the Darlington circuit 41, and the areas of the N-type epitaxial layers of the transistors QP11 and QN11, which are provided to the compensating circuit 42, are identical. However, by so arranging that S1<S3 and S2<S4 are satisfied, that is, by so arranging that the areas of the N-type epitaxial layers of the transistors QP11 and QN11 are larger than the areas of the N-type epitaxial layers of the transistors QP1 and QN1, it is possible to ensure that the photoelectric leak currents are compensated even if the photoelectric leak currents and the compensating current Io are not equal due to, for example, a mismatch of the elements.

Here, as an example of an arrangement similar to that of the present invention, Fig. 2 illustrates a photoelectric current compensating circuit described in Japanese Publication for Unexamined Patent, *Tokukaihei* No. 3-292775 (Publication Date: December 24, 1991). In this related art, sections corresponding to those in Fig. 1 are labeled with the same referential numerals. In this related art, a compensating circuit 40 including a PNP transistor QP11 having a single output stage compensates, by absorbing a compensating current Io, for a photoelectric leak current Ileak of a PNP transistor QP1 having a single output stage.

This related art is similar to the present invention in that it attains a higher accuracy by using an emitter current of the PNP transistor QP11, instead of a base current, in compensating for a collector current of the PNP transistor QP1. However, this related art is incompatible with the Darlington circuit 41. It is difficult to compensate, with a high accuracy, for the photoelectric leak current I2 of the NPN transistor QN1 by using only the PNP transistor QP11.

Fig. 3 is a block diagram illustrating an electric discharge circuit 50 of a wave detecting circuit as one example in which such Darlington circuit 41 and compensating 42 as described above are used. Fig. 4 is a block diagram illustrating an arrangement of a receiving device 51 of an infrared remote control, the receiving device 51 using the electric discharge circuit 50 as a wave detecting circuit 58. The receiving device 51 converts an infrared

transmission code signal into a photoelectric current signal Iin by using an external photodiode 52. After that, the receiving device 51 inputs the photoelectric current signal Iin to a receiving chip 53, which is an integrated circuit. The receiving device 51 then demodulates the photoelectric current signal Iin by using the receiving chip 53, so as to obtain an output signal RXOUT, and outputs the output signal RXOUT to a microcomputer or the like that controls an electronic device. The receiving chip 53 is an example of an optical signal circuit provided in proximity with the photodiode 52, which is a light-electricity conversion element. The infrared radiation signal is an ASK signal modulated by a predetermined carrier of approximately 30kHz to 60kHz, for example.

In the receiving chip 53, the photoelectric current signal Iin is sequentially amplified by a first stage amplifier (HA) 54, a second stage amplifier (2ndAMP) 55, and a third stage amplifier (3rdAMP) 56. By a band pass filter (BPF) 57, which is conformed to a frequency of the carrier, a carrier component Sig is extracted. Then, by the wave detecting circuit 58, which is a next stage, the carrier component Sig is detected at a carrier detection level Det. Thereafter, by an integration circuit 59, an integration is performed with respect to a time period in which the carrier is present. An integration output Int, which is obtained by the integration, is compared with a predetermined threshold level by a hysteresis comparator 60, so as to make a judgment as to whether or not the

carrier is present. Then, a result of the judgment is digitally outputted as the output signal RXOUT.

On an output side of the first stage amplifier 54, a low pass filter 61 is provided. The low pass filter 61 detects a direct current level of a fluorescent light and sunlight, and filters out, from an output of the first stage amplifier 54, a component corresponding to the direct current level before the second stage amplifier 55, which is a next stage, amplifies an output of the low pass filter 61. Therefore, an influence of noises caused by the fluorescent light, the sunlight, and the like, is reduced to some degree. Moreover, there is provided an ABCC circuit 62 associated with the first stage amplifier 54. In accordance with the output of the low pass filter 61, the ABCC circuit 62 controls a direct current bias of the first stage amplifier 54. There is further provided an fo trimming circuit 63 associated with the band pass filter 57. When a pulse current is applied to zener diodes (not shown) between terminals TRM1 to TRM 5, which are extended from connecting points of resistors (not shown) that are serially connected in the fo trimming circuit 63, the zener diodes are trimmed. In this way, a center frequency of the band pass filter 57 is adjusted.

The electric discharge circuit 50 constitutes a collector grounding circuit. An input terminal of the electric discharge circuit 50 is connected to the base of the NPN transistor QN1, and is connected to a capacitor C1 for removing noises. An output terminal of the electric discharge circuit 50 is connected to the

collector of the PNP transistor QP1, and is grounded via a constant current source F1. The electric discharge circuit 50 is used as an output buffer of the wave detecting circuit 58. Usually, a next-stage circuit has a higher input impedance. Therefore, an output voltage V1 of the electric discharge circuit 50 varies in accordance with a difference between a current flowing from the PNP transistor QP1 and the constant current I1 absorbed by the constant current source F1. Specifically, if Ileak>Io+I1, the output voltage V1 increases. However, by so arranging that Ileak<Io+I1, the output voltage V1 is prevented from increasing, and a compensating current, which is an excess current, flows in the PNP transistors QP1 and QP11.

As described above, the Darlington circuit 41 and the compensating circuit 42 of the present invention are capable of compensating for the photoelectric leak current Ileak, thereby attaining a high input impedance, and can therefore be suitably used, for example, for a wave detecting circuit having a built-in capacitor C1 that requires a high input impedance.

With reference to Fig. 5, the following describes another embodiment of the present invention.

Fig. 5 is an electrical diagram of another embodiment of the present invention. In this circuit, an NPN transistor (fifth NPN transistor) QN2 is added, as a compensation target circuit, to a Darlington circuit 41 having the same arrangement as that of the circuit in Fig. 1. A base of the NPN transistor QN2 receives the

collector current of the PNP transistor QP1. By thus arranging the circuit to be three-staged, the input impedance is further increased.

Here, the foregoing effects are attained if $S1 \leq S3$ and $S2 \leq S4$ are satisfied. In this case, an output current Iout is given by:

$$Iout = hfe(n) \times [hfe(p) \times \{S1 \times Ipd(p) + S2 \times Ipd(n)\} - hfe(p) \times \{S3 \times Ipd(p) + S4 \times Ipd(n)\}] \quad \ldots(10).$$

In the circuit where the input impedance is increased by thus further providing the NPN transistor QN2 as a next stage of the PNP transistor QP1, the difference between the photoelectric leak current Ileak and the compensating current Io is multiplied by hfe(n) of the NPN transistor QN2. However, the difference can be eliminated by so arranging that the compensating current is no smaller than the photoelectric leak current. Therefore, the influence of the photoelectric leak current Ileak can be eliminated even if the amplification rate is high.

Furthermore, even if three or more stages are provided, the influence of the photoelectric leak current Ileak can be decreased by similarly providing the photoelectric leak current compensating circuit. Although the present invention is particularly effective when laterally structured transistors are used, the present invention may be applied to vertically structured transistors.

As described above, a photoelectric leak current compensating circuit of the present invention is a photoelectric leak current compensating circuit for compensating for a photoelectric leak current generated in a Darlington circuit, which is provided in

an integrated circuit, including a first PNP transistor and a second NPN transistor whose collector is connected to a base of the first PNP transistor, the photoelectric leak current compensating circuit including a Darlington circuit, including a third PNP transistor, whose emitter is connected to a collector of the first PNP transistor and whose collector is grounded, for compensating for the photoelectric leak current by absorbing a collector current of the first PNP transistor; and a diode-structured fourth NPN transistor whose collector is connected to a base of the third PNP transistor and whose base and emitter are connected to each other.

According to this arrangement, in order to compensate for the photoelectric leak current of the Darlington circuit (i) which is provided in the integrated circuit, (ii) in which the base of the first PNP transistor is connected to the collector of the second NPN transistor, and (iii) which is suitable for improving an input impedance, the compensating circuit includes the Darlington circuit including the third PNP transistor, whose emitter is connected to the collector of the first PNP transistor and whose collector is grounded, and the diode-structured fourth NPN transistor whose collector is connected to the base of the third PNP transistor and whose base and emitter are connected to each other, the photoelectric leak current being compensated by absorbing, from the emitter of the third PNP transistor, the collector current of the first PNP transistor.

If the photoelectric leak current is compensated by using a

base current of the first PNP transistor, as shown in Fig. 13, a current mirror circuit and the like is needed in order to add a compensating current to the base current. Therefore, the number of elements is increased, thereby increasing the chip area. In contrast, with the foregoing arrangement, the photoelectric leak current is compensated by using the collector current. This makes it possible to compensate for the photoelectric leak current with a high accuracy without increasing the chip area, by so disposing the compensating circuit and the Darlington circuit that the compensating circuit and the Darlington circuit are equally influenced by light (e.g. by disposing the compensating circuit and the Darlington circuit on the same integrated circuit and in proximity with each other), the Darlington circuit including the third PNP transistor and the fourth NPN transistor, which have N-type epitaxial layers of substantially identical areas.

Moreover, it is preferable that a photoelectric leak current compensating circuit of the present invention is the photoelectric leak current compensating circuit, wherein $S1 \leq S3$, and $S2 \leq S4$ are satisfied, where S1 and S2 are areas of N-type epitaxial layers of the first PNP transistor and the second NPN transistor, respectively, and S3 and S4 are areas of N-type epitaxial layers of the third PNP transistor and the fourth NPN transistor, respectively.

By thus arranging the area S1 of the N-type epitaxial layer (base scattering region) of the first PNP transistor, the area S2 of the N-type epitaxial layer (collector scattering region) of the second

NPN transistor, the area S3 of the N-type epitaxial layer (base scattering region) of the third PNP transistor, and the area S4 of the N-type epitaxial layer (collector scattering region) of the fourth NPN transistor, it is possible to obtain a compensating current that is no smaller than the photoelectric leak current, thereby ensuring that the photoelectric leak current is compensated.

Especially, by so arranging that S1<S3, and S2<S4, it is possible to ensure that the photoelectric leak current is compensated, even if the photoelectric leak current and the compensating current are not equal due to, for example, a mismatch of elements.

Moreover, it is preferable that a photoelectric leak current compensating circuit of the present invention is a photoelectric leak current compensating circuit, further comprising a fifth NPN transistor whose base receives the collector current of the first PNP transistor.

With this arrangement, in the circuit where the input impedance is increased by thus further providing the fifth NPN transistor as a next stage of the first PNP transistor, the difference between the photoelectric leak current and the compensating current is multiplied by hfe of the fifth NPN transistor. However, the difference can be eliminated by so arranging that the compensating current is no smaller than the photoelectric leak current. Therefore, the influence of the photoelectric leak current can be eliminated even if the amplification rate is high.

Moreover, it is preferable that a photoelectric leak current compensating circuit of the present invention is the photoelectric leak current compensating circuit, wherein the collector of the first PNP transistor is grounded via a constant current source, and a sum of (i) a constant current of the constant current source and (ii) the collector current, which is absorbed by the third PNP transistor, of the first PNP transistor is larger than the photoelectric leak current.

According to this arrangement, the sum of (i) the constant current of the constant current source and (ii) the collector current, which is absorbed by the third PNP transistor, of the first PNP transistor is larger than the photoelectric leak current. Therefore, it is possible to prevent an increase of an output voltage of an output terminal connected to the collector of the first PNP transistor, the output voltage varying in accordance with the difference between the current flowing from the first PNP transistor and the constant current of the constant current source.

Moreover, it is preferable that a photoelectric leak current compensating circuit of the present invention is the photoelectric leak current compensating circuit, wherein the transistors are laterally structured.

With this arrangement, the present invention is particularly effective because, in laterally structured transistors, N-type epitaxial layers, which are base scattering regions in PNP transistors and collector scattering regions in NPN transistors, are

widely exposed.

Moreover, an optical signal circuit of the present invention is an optical signal circuit, comprising the photoelectric leak current compensating circuit.

Therefore, the foregoing effects are attained in the optical signal circuit.

The invention being thus described, it will be obvious that the same may be varied in many ways. Such variations are not to be regarded as a departure from the spirit and scope of the invention, and all such modifications as would be obvious to one skilled in the art are intended to be included within the scope of the following claims.